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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,293	12/15/2003	Michael Andrew de Rooij	132853	1786

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GENERAL ELECTRIC COMPANY
GLOBAL RESEARCH
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EXAMINER	
SMITH, JACKSON R	

ART UNIT	PAPER NUMBER
1709	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,293	DE ROOIJ ET AL.	
	Examiner	Art Unit	
	Jack Smith	1709	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 12/15/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 6, 7 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steigerwald (US Patent 4,424,557) in view of Suelzle et al. (US Patent 5,397,927).

As to claim 1, Steigerwald discloses a power converter system in Figure 1 comprising: a photovoltaic array (solar array, 11); an inverter electrically coupled to said photovoltaic array (full bridge current-controlled inverter, 1) to generate an output current for energizing a load connected to said inverter and to a mains grid supply voltage (i.e., "Utility Grid," labeled in the figure). Steigerwald further discloses a controller (control, 25) that provides switching signals to the transistors in the inverter (column 2, lines 45-47) via current band PWM (abstract). What Steigerwald fails to disclose is that the controller has the circuitry recited in this claim that is meant to reduce harmonics.

Suelzle et al., disclose circuitry that comprises a controller and a filter (Active Filter, 16, Figure 1) for use with an AC power line (abstract, first sentence), such as would be created by the photovoltaic array coupled to an inverter of Steigerwald. As

Suelzle et al. explain in column 3 lines 30-42, this circuit uses current injection to reduce harmonics (i.e., non-fundamental frequency voltages) in the power line. Said filter includes a first circuit coupled to receive a load current to measure a harmonic current in said load current (circuit including the "first voltage sensing circuit" and the "current sensing transducer", 20, junction, 24, and notch filter, 26, in Figure 2 and described in column 4 lines 30-35), a second circuit (the circuit including the "second voltage sensing circuit" as well as gain controller, 32, and bandpass filter, 39, Figure 2) to generate a fundamental reference drawn by said load (input power control signal, V10) ; and a third circuit (output circuit, including junction, 28, and output injection current, I_1) for combining (at junction, 28) the measured harmonic current (current from notch filter, 26, at V5 input to junction 28) and said fundamental reference (V10) to generate a command output signal for generating the output current (output current, I_1) for energizing the load connected to said AC power line (as shown in Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to add the circuitry in the filter of Suelzle et al. to the controller of Steigerwald in the photovoltaic converter system of Steigerwald in order to reduce harmonics. The output of the controller of Suelzle et al. would be coupled to the inverter of Steigerwald via standard pulse width modulation techniques, such as those taught by Steigerwald, known by those of ordinary skill in the art.

As to claim 2, the first circuit of Suelzle et al. ("first voltage sensing circuit", Figure 1) in the modified device of Steigerwald comprises a notch filter (notch filter, 26) configured to pass harmonics present in the load current (as explained in column 4,

lines 42-43, the notch filter is configured to "remove the fundamental frequency component" of the load current, I_L).

As to claim 6, Steigerwald discloses a photovoltaic array (solar array, 11); an inverter electrically coupled to said photovoltaic array (full bridge current-controlled inverter to generate an output current for energizing a load connected to said inverter and to a mains grid supply voltage (i.e., "Utility Grid," labeled in the figure). Steigerwald further discloses a controller (control, 25) that provides switching signals to the transistors in the inverter (column 2, lines 45-47) via current band PWM (abstract). What Steigerwald fails to disclose is that the controller has the circuitry recited in this claim that is meant to reduce harmonics.

Suelzle et al., disclose circuitry that comprises a controller and a filter (Active Filter, 16, Figure 1) for use with an AC power line (abstract, first sentence), such as would be created by the photovoltaic array coupled to an inverter of Steigerwald. As Suelzle et al. explain in column 3 lines 30-42, this circuit uses current injection to reduce harmonics (i.e., non-fundamental frequency voltages) in the power line. Said controller includes a first circuit coupled to receive a load current to measure a harmonic current in said load current (circuit including the "first voltage sensing circuit" and the "current sensing transducer", 20, junction, 24, and notch filter, 26, in Figure 2 and described in column 4 lines 30-35), a second circuit (the circuit including the "second voltage sensing circuit" as well as gain controller, 32, and bandpass filter, 39, Figure 2) to generate a fundamental reference drawn by said load (input power control signal, V10) ; and a third circuit (Output circuit, including junction, 28, and output injection current, I_1) for

combining (at junction, 28) the measured harmonic current (current from notch filter, 26, at V5 input to junction 28) and said fundamental reference (V10) to generate a command output signal for generating the output current (output current, I1) for energizing the load connected to said AC power line (as shown in Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to add the circuitry in the filter of Suelzle et al. to the controller of Steigerwald in the photovoltaic converter system of Steigerwald in order to reduce harmonics. The output of the controller of Suelzle et al. would be coupled to the inverter of Steigerwald via standard pulse width modulation techniques, such as those taught by Steigerwald, known by those of ordinary skill in the art.

As to claim 7, the first circuit of Suelzle et al. ("first voltage sensing circuit", Figure 1) in the modified device of Steigerwald comprises a notch filter (notch filter, 26) configured to pass harmonics present in the load current (as explained in column 4, lines 42-43, the notch filter is configured to "remove the fundamental frequency component" of the load current, I_L).

As to claim 11, Steigerwald discloses a method for controlling a power converter system ("method and apparatus for switching full bridge current controlled power converter", column 1, lines 5-6). As shown in Figure 1 and described in column 1 lines 30-34, said method includes coupling a photovoltaic array (solar array, 11) to an inverter electrically coupled to said photovoltaic array (full bridge current-controlled inverter to generate an output current for energizing a load connected to said inverter and to a mains grid supply voltage (i.e., as part of the "Utility Grid," labeled in the figure). What

Steigerwald fails to disclose is the method for measuring a load current, receiving that load current and using it to generate a command output signal for energizing the load connected to said inverter.

Suelzle et al., disclose a method for controlling an AC power line (column 3, lines 16-18) to generate an output current (output current, I_1) for energizing a load connected to said AC power line (14). As Suelzle et al. explain in column 3 lines 30-42, this circuit uses current injection to reduce harmonic (i.e., non-fundamental frequency voltages) in the power line. The method of Suelzle et al. comprises: receiving a load current (the method by which the "current sensing transducer", shown in Figure 2 receives the current is described in column 4 lines 30-35) to measure a harmonic current (as described in column 4, lines 42-43, notch filter 26 is used to remove the fundamental frequency component all leave only the harmonic components and this signal is then provided as a measure of the harmonic components to junction 28) in said load current generating a fundamental reference (i.e., that supplied to the junction, 28, by the band pass filter, 39) drawn by said load; and combining the measured harmonic current (supplied to junction 28 by notch filter 26) and said fundamental reference. Suelzle et al. describe how the harmonics from V5 and the fundamental reference from V10 are combined in junction 28 in column 44-47 and provided as a command output signal (V6) that is inputted to the control mechanism (trans-conductance amplifier, 18) which uses it to generate the output current (injection current I_1) as described in first in column 4, lines 24-25 and later in column 4, lines 47-50. That this latter step energizes the load (14) connected to the AC power line (12) follows from the fact that the load is connected

to this power line (as shown in Figure 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to add the method of controlling an AC power line taught by Suelzle et al. to the method for controlling a power converter taught by in order to reduce harmonics. The output of the controller of Suelzle et al. would be coupled to the inverter of Steigerwald via standard pulse width modulation techniques, such as those taught by Steigerwald, known by those of ordinary skill in the art.

As to claim 12, in the combined method of Steigerwald involves receiving of the load current comprises processing said load current to pass harmonics present in said load current (Suelzle et al. describe in column 4, lines 42-43). Specifically, the notch filter 26 is used to remove the fundamental frequency component all leave only the harmonic components and this signal is then provided as a measure of the harmonic components to junction 28.

As to claim 13, the details of generating and using the fundamental reference in the combined method of Steigerwald is described by Suelzle et al. In column 4 lines 30-48, Suelzle et al. explain the steps for generating fundamental reference (V10) by using the second voltage sensing circuit (30) to receiving a supply voltage (V1, input to 30) to generate a sinusoid (V7 at the X terminal of analog multiplier, 32). As Suelzle et al. explain in column 5, line 30-35, the sinusoid is ultimately fed to a band pass filter (39) that ensures that the fundamental reference produced (V10) has the frequency (f_0) of said supply voltage.

As to claim 14, the details of generating and using the fundamental reference in the combined method of Steigerwald is described by Suelzle et al. In column 6, lines 37-

41, Suelzle et al. explain how the fundamental reference (the output voltage at the Z port of 32 which is sent through bandpass filter, 39, to become V10 as instructed in Figure 2) is generated by using gain controller (32) to mix sinusoid (V7) and a signal indicative of the magnitude of current available from the photovoltaic array (V9, whose generation relates to current I_L as well as reference voltage VREF) for generating the fundamental reference (V10) drawn by said load.

3. Claims 3 , 4, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steigerwald (US Patent 4,424,557) in view of Suelzle et al. (US Patent 5,397,927) and in further view of O'Sullivan et al. (US Patent 5,929.538).

As to claims 3 and 8, the combined device of Steigerwald and Suelzle et al. meets all the limitations of claims 1 and 6 above. The second circuit supplied by Suelzle et al. to this combined device further comprises a loop (second voltage sensing circuit, Figure 2) coupled to receive said supply voltage (V1, as shown in the figure) and generate a sinusoid (V7 at the X terminal of analog multiplier, 32) that corresponds to the frequency of said supply voltage. What Suelzle et al. as combined with Steigerwald fails to teach is the use of a phase-lock loop in the second circuit in order to generate an actual fundamental current reference that is synchronized with the supply voltage.

O'Sullivan et al. disclose a multimode power processor (title) that can be used as an inverter for delivering power from a generator to a power grid (abstract). One embodiment of said power processor includes a control block (Figure 22) which inputs the generator voltage to a digital controller via a phase lock loop (PLL, middle of Figure 22). As O'Sullivan et al. explain in column 22, lines 27-30, that the use of this phase

locked loop allows the generator to communicate with the controller such that desired waveforms may be synchronized with the generator voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the phase lock loop of O'Sullivan et al. to the loop (second voltage sensing circuit, Figure 2) of the modified device of Steigerwald in order to synchronize the sinusoid (V7) received by said loop with the supply voltage (V1).

As to claims 4 and 9, the second circuit of Suelzle et al. provided to the combined device of Steigerwald further comprises a mixer (analog multiplier, 32) configured to receive said sinusoid (32 receives the sinusoid, V7, at input X) and a signal indicative of the magnitude of current available from the AC power line (i.e., V9). The response of the circuit (i.e., the second circuit that includes mixer, 32) with respect to the magnitude of the voltage on the AC power line is described in column 7, lines 40-55. Finally, as Suelzle et al. explain in column 6, lines 43-45, these signals are combined by mixer (32) and sent through band pass filter 39 in order to provide a fundamental reference (i.e., "to produce control signal V10 which is thus proportional to the fundamental frequency component of V1 on the AC power line 12").

4. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steigerwald (US Patent 4,424,557) in view of Suelzle et al. (US Patent 5,397,927) and in further view of Hopkins ("Partitioning Digitally Programmable Power-Control for Applications to Ballasts").

Steigerwald and Suelzle et al. are cited as above for claims 1 and 6. What the modified device of Steigerwald fails to provide is that the controller may be selected

from the group consisting of a micro-controller, a Field Programmable Gate Array device and an Application Specific Integrated Circuit device.

Hopkins discusses various methods, including digital methods, for controlling power electronic circuits (introduction, first sentence). In the fourth paragraph of the introduction, Hopkins explains that the use of analog ASIC's to control power in such systems can lower system costs. It would have been obvious to one of ordinary skill in the art at the time of the invention to fashion the power controller of the modified device of Steigerwald into an ASIC in the manner taught by Hopkins in order to lower system costs.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Smith whose telephone number is (571) 272-9814. The examiner can normally be reached on 7:30 a.m. - 5:00 p.m., Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexa Neckel can be reached on (571) 272-1446. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

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JRS

/JRS/

/Alexa Neckel/

ALEXA D. NECKEL
SUPERVISORY PATENT EXAMINER